CS6303 COMPUTER ARCHITECTURE L T P C
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UNIT I OVERVIEW & INSTRUCTIONS 9

Eight ideas – Components of a computer system – Technology – Performance – Power wall – Uniprocessors to multiprocessors; Instructions – operations and operands – representing instructions– Logical operations – control operations – Addressing and addressing modes.

UNIT II ARITHMETIC OPERATIONS 7

ALU - Addition and subtraction – Multiplication – Division – Floating Point operations – Sub word parallelism.

UNIT III PROCESSOR AND CONTROL UNIT 11

Basic MIPS implementation – Building data path – Control Implementation scheme – Pipelining –Pipelined datapath and control – Handling Data hazards & Control hazards – Exceptions.

UNIT IV PARALLELISM 9

Instruction-level-parallelism – Parallel processing challenges – Flynn's classification – Hardware multithreading – Multicore processors

UNIT V MEMORY AND I/O SYSTEMS 9

Memory hierarchy - Memory technologies – Cache basics – Measuring and improving cache performance - Virtual memory, TLBs - Input/output system, programmed I/O, DMA and interrupts, I/O processors.

TOTAL: 45 PERIODS

TEXT BOOK:

1. David A. Patterson and John L. Hennessey, “Computer organization and design’, Morgan Kauffman / Elsevier, Fifth edition, 2014.

REFERENCES:

1. V.Carl Hamacher, Zvonko G. Varanesic and Safat G. Zaky, “Computer Organisation“, VI th edition, Mc Graw-Hill Inc, 2012.
2. William Stallings “Computer Organization and Architecture” , Seventh Edition , Pearson Education, 2006.
3. Vincent P. Heuring, Harry F. Jordan, “Computer System Architecture”, Second Edition,Pearson Education, 2005.
4. Govindarajalu, “Computer Architecture and Organization, Design Principles and Applications", first edition, Tata McGraw Hill, New Delhi, 2005.
5. John P. Hayes, “Computer Architecture and Organization”, Third Edition, Tata Mc Graw Hill,1998.
6. http://nptel.ac.in/.

Description:

In electronics engineering and computer engineering, **computer architecture** is a set of disciplines that describes a computer system by specifying its parts and their relations.

For example, at a high level, computer architecture may be concerned with how the central processing unit (CPU) acts and how it uses computer memory. Some fashionable computer architectures include cluster computing and non-uniform memory access.

Computer architects use computers to design new computers. Emulation software can run programs written in a proposed instruction set. While the design is very easy to change at this stage, compiler designers often collaborate with the architects, suggesting improvements in the instruction set. Modern emulators may measure time in clock cycles: estimate energy consumption in joules, and give realistic estimates of code size in bytes. These affect the convenience of the user, the life of a battery, and the size and expense of the computer's largest physical part: its memory. That is, they help to estimate the value of a computer design.

Objectives:

- To make students understand the basic structure and operation of digital computer.
- To understand the hardware-software interface.
- To familiarize the students with arithmetic and logic unit and implementation of fixed point and floating-point arithmetic operations.
- To expose the students to the concept of pipelining.
- To familiarize the students with hierarchical memory system including cache memories and virtual memory.
- To expose the students with different ways of communicating with I/O devices and standard I/O interfaces.

Outcomes:

At the end of the course, the student should be able to:

- Design arithmetic and logic unit.
- Design and analyse pipelined control units
- Evaluate performance of memory systems.
- Understand parallel processing architectures.

WEEKS	HOURS	LECTURE TOPICS	READING
I		**UNIT I OVERVIEW & INSTRUCTIONS**	
	1	Eight ideas **(AV Class)**	T1
	2	Components of a computer system	T1
	3	Technology – Performance	T1
	4	Power wall – Uniprocessors to multiprocessors	T1
II	5	Instructions – operations and operands	T1
	6	Representing instructions	T1
	7	Logical operations	T1
	8	Control operations	T1
III	9,10	Addressing and addressing modes**(AV Class)**	
		UNIT II ARITHMETIC OPERATIONS	
	10	ALU**(AV Class)**	T1
	11	Addition and subtraction**(AV Class)**	T1
IV	12	Multiplication	T1
	13	Division	T1
	14,15	Floating Point operations**(AV Class)**	T1
V	16,17	Subword parallelism.	T1
		UNIT III PROCESSOR AND CONTROL UNIT	
	18,19	Basic MIPS implementation	T1
	20	Building datapath	T1
VI	21	Control Implementation scheme	T1
	22,23	Pipelining**(AV Class)**	T1
	24,25	Pipelined datapath and control**(AV Class)**	T1
	26-28	Handling Data hazards & Control hazards – Exceptions**(AV Class)**	T1
VII		**UNIT IV PARALLELISM**	
	29,30	Instruction-level-parallelism**(AV Class)**	T1
	31	Parallel processing challenges	T1
VIII	32-33	Flynn's classification**(AV Class)**	T1
	34,35	Hardware multithreading	T1
	36,37	Multicore processors	T1
IX		**UNIT V MEMORY AND I/O SYSTEMS**	
	38	Memory hierarchy**(AV Class)**	T1
	39	Memory technologies	T1
	40	Cache basics	T1
X	41	Measuring and improving cache performance	T1
	42,43	Virtual memory, TLBs**(AV Class)**	T1
	44	Input/output system, programmed I/O**(AV Class)**	T1
XI	45,46	DMA and interrupts**(AV Class)**	T1
	47	I/O processors**(AV Class)**	T1

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